Dr. Balwinder Singh

Designation: Coordinator & Senior Engineer

Contact Information:

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Educational Background:

- 2009-2014: Ph.D. in Low Power VLSI Testing (Guru Nanak Dev University, Amritsar India)
- 2002-2004: M. Tech in Microelectronics , Panjab University Chandigarh India
- 1998-2002: B.Tech in Electronics & Instrumentation Engg (National Institute of Technology Jalandhar, India)

Positions Held:

- July 2010 – till date : working as Senior Engineer & Coordinator ACS Division , Centre for Development of Advanced Computing (C-DAC), Mohali
- 2006- 2010: Worked as Design Engineer , Centre for Development of Advanced Computing (C-DAC), Mohali
- July 2004 – July 2004: worked as Lecturer in Sant Baba Bhag Singh Institute of Engg & Tech. Jalandhar

Research Interest:

- Low power VLSI Design and Testing
- Digital IP cores and analog modules
- Sensor and MEMS design and modeling
- FPGA based embedded systems,
- Image Processing for Embedded systems

Professional Memberships:

- Member of VLSI SOCIETY OF INDIA
- Member of Indian Microelectronics society (IMS) founded jointly by SCL, CSIO and Panjab University Chandigarh.
- Member of IEEE

Other Academic Activities:

1. Coordinator, Academic & Consultancy Services Division, C-DAC, Mohali.
2. Initiated & Design course curriculum of new M.Tech programs viz., Information technology, Embedded System, and Electronics Product Design & Technology.
3. Member, Board of Studies,
    - Punjab Technical University, Jalandhar,
    - Bhara University Solan
    - Chitkara University Rajpura

4. Member, Library Committee, C-DAC, Mohali.
5. Member, Material Write-Off Committee, C-DAC, Mohali.
6. Course Coordinator, Short Term Courses, C-DAC, Mohali.
7. Paper setter for
    - M. Tech Microelectronics , Panjab University, Chandigarh
    - M. Tech VLSI Chandigarh University , Gharuan, Mohali
    - M. Tech VLSI Design Bhara University Solan

8. External examiner for evaluation of M.Tech Thesis at Panjab Technical University , Jalandhar
9. External Examiner for Evaluation of B.E. (Major projects) and M.E. (Thesis).
10. Establishment and Modernization of various M.Tech Labs at C-DAC Mohali.

Software /Tools Exposure

- Cadence Front end & Back end flow
- Xilinx Webpack ISE, Model Sim, Isim, Turbo tester ,Atlanta
- Cadence Tools
- MATLAB
- Tannar tools
- AVR studio

Subject Teaching Graduate level

- instrumentation Engg ,
- Digital Electronics,
- Microprocessor,
- Electronics Devices and Circuits
- Linear control system

Post graduate level

- VLSI Technology ,
- System on Chip ,
- Embedded system design,
- Advanced DSP
- VLSI Design concepts

Selected Publications

Conferences and Workshops

[1] Balwinder Singh, Arun Khosla and Sukhleen Bindra(2009). **Power Optimization for Linear feedback Shift Register (LFSR) for BIST**, *IEEE International Advance computing Conference, TIET Patiala March 09 Page(s): 311-314* http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=4809027

[2] Pawan Verma Harpreet Kaur, Mandeep singh, Balwinder Singh, "**VHDL Implementation of FFT/IFFT Blocks for OFDM**", *International Conference on Advances in Recent Technologies in Communication and Computing held at* ***Kottayam, Kerala 2009*** pp 186-188. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5327801

[3] R.P.P.Singh.Parveen Kumar,Performance Analysis Of Fast Adders Using VHDL *International Conference on Advances in Recent Technologies in Communication and Computing held at* ***Kottayam,2009*** *http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5327807*

[4] Singh, Balwinder and Kaur, Harpreet and Monga, Himanshu **"FPGA Implementation of AES Co-processor in Counter Mode**" Information Processing and Management Communications in Computer and Information Science Springer Verilag, New York Volume 70, 2010 491-*496* *http://link.springer.com/chapter/10.1007% 2F978-3-642-12214-9_85*

[5] Paramjot Saini, Mandeep Singh and Balwinder Singh "**VHDL Implementation of PCI Bus Arbiter Using Arbitration Algorithms** "Contemporary Computing Communications in Computer and Information Science, 2011, Volume 168, Part 4, 559-560, Springer Verilag, New York *http://link.springer.com/chapter/10.1007/978-3-642-22606-9_62*

[6] Gurinder Pal Singh and Balwinder Singh "**Simulink Library Development and Implementation for VLSI Testing in Matlab"** Communications in Computer and Information Science Volume 169, Part 2, 233-240,published by Springer Berlin Heidelberg , New York http://link.springer.com/chapter/10.1007/978-3-642-22577-2_31

[7] Balwinder Singh , Sukhleen Bindra Narang, and Arun Khosla(2012) **Area Overhead and Power Analysis of March Algorithms for Memory BIST**, Procedia Engineering Volume 30 Page(s): 930 – 93 http://www.sciencedirect.com/science/article/pii/S1877705812009575

[8] Gurinder Pal ,Padma devi , Balwinder Singh "**Low power optimized array multiplier with reduced area"** Communications in Computer and Information Science Volume 169, Part 2, 224-232 published by Springer Berlin Heidelberg , New York http://link.springer.com/chapter/10.1007%2F978-3-642-22577-2_30

[9] Balwinder singh , Sukhleen Bindra Narang, and Arun Khosla(2010) Modeling and Simulation of Efficient March Algorithm for Memory Testing **Contemporary Computing Communications in Computer and Information Science, 2**010, Volume 95, Part 2, Page(s): 96-107 published by Springer Berlin Heidelberg , New York http://link.springer.com/chapter/10.1007/978-3-642-14825-5_9

[10] Singh, Balwinder, Sukhleen Bindra Narang, and Arun Khosla. "Analysis of Cellular Automata and Genetic Algorithm based Test Pattern Generators for Built In Self Test." Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications (BIC-TA 2012). Springer India, 2013. http://link.springer.com/chapter/10.1007/978-81-322-1038-2_36

Books / Book Chapters:

Books

[11] Balwinder Singh, Ashish Dixit "Analog Electronics "2007 , Laxmi Publications (P) Ltd,113, Golden House, Daryaganj, New Delhi - 110002, India

Available at : http://www.laxmipublications.com/servlet/lpdispinfo?offset=0&text1=balwinder&searchtype=Keywords

[12] Balwinder Singh, Ashish Dixit, Balwant Raj " Electronics Devices and circuits "2008 [ISBN : 978-81-318-0691-3], Laxmi Publications (P) Ltd,113, Golden House, Daryaganj , New Delhi - 110002, India

http://www.laxmipublications.com/servlet/lpdispinfo?offset=0&text1=balwinder&searchtype=Keywords

Balwinder Singh. Dr. B.RAJ. Ashish Dixit " VLSI Fabrication Technology:" : Laxmi Publications(P) Ltd, New Delhi ISBN 978-93-81159-60-6 Edition: First, 2013
http://www.laxmipublications.com/servlet/lpdispinfo?offset=0&text1=balwinder&searchtype=Keywords

[13] Gurinder pal Singh, Balwinder Singh "Simulink Library Development and Implementation for VLSI Testing (MATLAB Concepts for VLSI Testing)" : ISBN-13: 978-3-659-13043-4 LAP Lambert Academic Publishing (2012-05-18)
https://www.lap-publishing.com/catalog/details/store/gb/book/978-3-659-13043-4/simulink-library-development-and-implementation-for-vlsi-testing?search=balwinder

International Journals

[14] Balwinder Singh ,Padma Devi Ashima Girdher , "Improved Carry Select Adder with Reduced Area and Low Power Consumption" , International Journal of Computer Applications Vol. 3(4),pp 14–18 June 2010

[15] Balwinder singh , Sukhleen Bindra Narang, and Arun Khosla(2011) Address Counter / Generators for Low Power Memory BIST, IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 4, No 1, July 2011 ISSN (Online): 1694-0814 Page(s): 561-567

[16] Balwinder singh , Sukhleen Bindra Narang, and Arun Khosla(2011)Particle Swarm Optimization Framework for Low Power Testing of VLSI Circuits, International Journal of Artificial Intelligence & Applications (IJAIA), Vol.2, No.3, July 2011 Page(s): 13-20

[17] Balwinder singh , Sukhleen Bindra Narang, and Arun Khosla(2011) MATLAB based Cost modeling for VLSI Testing ,The Research Bulliten of Jorden, ACM,Volume 2 Issue 3 sepetmber 2011 Page(s): 95-99

[18] Balwinder Singh, Arun Khosla , " Low Power Bus Encoding Techniques for Memory Testing" Microelectronics and Solid State Electronics 2 (3), 45-51

[19] B Singh, SB Narang, A Khosla "Test Power Optimization with Reordering Of Genetic Test Vectors For VLSI Circuits" Acta Technica Napocensis. Electronica-Telecomunicatii 53 (2),

[20] Shikha Kakar, Balwinder Singh, and Arun Khosla , Implementation of BIST Capability using LFSR Techniques in UART, International Journal of Recent Trends in Engineering, Issue. 1, Vol. 1(3), May 2009 pp-301-304

[21] Vijender Saini, Balwinder Singh, and Rekha Devi, Area Optimization of FIR Filter and its Implementation on FPGA International Journal of Recent Trends in Engineering, Issue. 1, Vol. 1(4), May 2009 pp- 55-58

[22] Raminder Preet Pal Singh,Parveen Kumar, Balwinder Singh, "Performance Analysis of 32 Bit Array Multiplier with a Carry Save Adder and with a Carry Look Ahead Adder" , International Journal of Recent Trends in Engineering, Issue. 1, Vol. 2, November 2009

[23] Gurinder Pal Singh and Balwinder Singh "Simulink Model For Controllability And Observability Of VLSI Circuits" Journal of Global Research in Computer Science Volume 1, No. 3, October 2010

[24] Amandeep Singh and Balwinder Singh "Microcontroller based Testing of Digital IP-Core" International Journal of VLSI Design and & Communication System, 2012, April Volume 3

[25] Ana Monga and Balwinder Singh "Finite State Machine Based Vending Machine Controller with Auto Billing Features" . International Journal of VLSI Design and & Communication System, 2012. Volume 3

[26] Amandeep Singh, Balwinder Singh "Design and Implementation Of Bit Transition Counter" Circuits and Systems: An International Journal (CSIJ), Vol. 1, No.1, January 2014

[27] Singh, Balwinder, Arun Khosla, and Sukhleen B. Narang. "Cost Modeling for SOC Modules Testing." International Journal of Information Engineering & Electronic Business 5.2 (2013).

[28] Sharma, Smriti, and Balwinder Singh. "Design and Performance Analysis Of ZBT SRAM Controller." International Journal of VLSI Design & Communication Systems 4.3 (2013).